Charge transport along and across integrated large-area graphene

M. A. Gluba, V. V. Brus, G. V. Troppenz, X. Zhang, K. Hinrichs, J. Rappich, and N. H. Nickel

Helmholtz-Zentrum Berlin für Materialien und Energie GmbH, Institut für Silizium Photovoltaik, Kekuléstr. 5, 12489 Berlin, Germany marc.gluba@helmholtz-berlin.de

Abstract

Pronounced polycrystallinity and substrate interaction lead to a remarkable variation of the effective mobility and the concentration of charge carriers in chemical vapor deposited graphene. The aim to integrate this material into large-area devices such as solar cells, displays, and touch screens creates a growing interest in the mechanisms of charge transport along and across embedded carbon monolayers. In this work we present a detailed investigation on charge transport in buried graphene encapsulated by silicon layers of different crystallinity, as well as the transport barriers across the graphene/silicon heterojunction.

To elucidate the governing charge-scattering mechanisms in buried layers, graphene was grown by chemical vapor deposition (CVD) and transferred to glass substrates. Subsequently, a capping layer of 300nm amorphous silicon was deposited and subsequently crystallized using electron beam crystallization (Fig 1a). Raman backscattering measurements performed at the buried interface confirm that the carbon monolayer withstands the deposition and crystallization process. Temperature dependent Hall-effect measurements reveal a significant impact of the crystallinity of the silicon layer on the transport properties of the encapsulated graphene electrode [1].

Vertical current transport was studied by transferring the CVD-grown graphene layers to hydrogenterminated single crystalline silicon. The heterojunction resembles the current-voltage characteristics of a Schottky contact and is sensitive to illumination with white light. However, the graphene/silicon heterojunction degrades noticeably and strong interface recombination impedes the extraction of photogenerated carriers. In contrast, methyl-passivated graphene/silicon heterojunctions (Fig. 1b) show remarkably low interface recombination with a defined transport barrier. The impact of this barrier as well as limiting mechanisms for lateral charge transport will be discussed in terms of graphene electrodes implemented in large-area silicon-based devices.

References

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Fig. 1. a) Schematic depiction of encapsulated graphene structures. b) Device structure of a lightsensitive graphene/silicon heterojunction. To reduce interface recombination the silicon surface was passivated using a monolayer of methyl groups.

Figures